S.D.COLLEGE OF ENGINEERING & TECHNOLOGY

Subject: VLSI **Subject Code: REC-702**

Branch: EC **Sem: VII**

Date of Given : **Date of Submission:**

ASSIGNMENT NO. 1

Q.1 Explain the structure and working of MOS transistor.

Q.2- Sketch a 2-Input CMOS NAND Gate & CMOS NOR Gate and also discuss the working.

Q.3- Sketch a complementary CMOS Gate computing Y= $\overline{(A+B+C).D}$

Q.4- Discuss the basic steps involved in fabrication process flow. Show supporting figure for each fabrication step.

Q.5- Write a short note on fabrication, packaging and testing of VLSI chip.

Q.6- Sketch a stick diagram for a CMOS 3-input NAND gate and also estimates the cell width and height.

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Date of Given : **Date of Submission:**

ASSIGNMENT NO. 2

Q.1- Define the following

a) Propagation delay time
b) Contamination delay time
c) Rise time
d) Fall time
e) Edge time
f) Instantaneous Power P(t)
g) Energy
h) average power

Q.2- Draw equivalent RC Circuit models for nMOS and pMOS transistors. Also draw the equivalent circuit for an inverter. Discuss briefly about effective resistance and gate and diffusion capacitance of RC delay model.

Q.3- Write a short note on the Elmore Delay.

Q.4- Explain linear delay model & the types of timing analysis delay models.

Q.5- What are the sources of power dissipation in CMOS circuits? Also discuss about the modes of power.

Q.6- What do you understand by logical effort of paths? Also give the limitations of logical effort.

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ASSIGNMENT NO. 3

Q.1Define interconnection .What are interconnecting models? Explain any two of them in brief.

Q.2 Explain the concept of RC Delay model. What are the limitations of logical effort .

Explain various types of power dissipation in CMOS circuits. Derive the expression for total power dissipation of a CMOS circuit

Q.3 Define Interconnect scaling. Draw and explain the working of Lumped RC-model for interconnects.

Q.4What are the various sources of power dissipation in CMOS circuits? Discuss in detail the variable threshold CMOS circuits.

Q.5 Calculate the delay involved in cascaded pass transistors. Discuss the Elmore Delay Narrate in detail about VLSI low power architectures with suitable diagram

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ASSIGNMENT NO. 4

Q.1Describe the working of three stage pseudo nMOS dynamic shift register driven with two- phase clocking giving its circuit

Q.2 i) Implement the Boolean function Y = AB + (C+D)(F+E)+GH using DOMINO CMOS logic.

(ii) Explain the term Voltage Boot Strapping in CMOS logic with suitable examples

iii) Explain NORA CMOS logic circuit with suitable example.

Q.4 Enlist the advantages of dynamic logic circuit over static logic circuit. Bring out the drawbacks of dynamic logic

Q.5Write short note on DRAM cell. Explain leakage and refresh operation in DRAM cells.

Differentiate between i) EEPROM and Flash memory ii) SRAM and DRAM.

Q.6Implement 2:1 MUX & 2 input EXOR Logic Gate using CMOS Transmission Gate.

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ASSIGNMENT NO. 5

Q.1 Explain the issues involved in Built-in Self Test (BIST) techniques in detail.

Q.2 Write a short note on

(i) Adiabatic Logic Circuit.

(ii) Explain the Scan Based Techniques.

(iii)Fault types and models

(iv) Controllability and observability

Q.3Describe leakage power dissipation and dynamic power dissipation..

Q.4 Define the terms- Defects, Errors and Faults. What is meant by Stuck-at-1(s-a-1) fault and Stuck-at-0(s-a-0) faults.

Q.5Why transistor scaling is of great importance in VLSI? Write down comparison between Constant field scaling and Constant voltage scaling.

Q.6 Briefly explains variable threshold CMOS (VTCMOS) circuit.

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